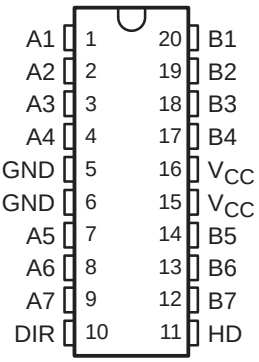
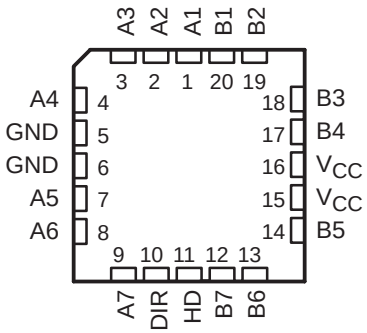
- **4.5-V to 5.5-V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 20 ns at 5 V**
- **3-State Outputs Directly Drive Bus Lines**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
- **Designed for the IEEE 1284-I (Level-1 Type) and IEEE 1284-II (Level-2 Type) Electrical Specifications**

SN54ACT1284 . . . J OR W PACKAGE
SN74ACT1284 . . . DB, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54ACT1284 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

The ’ACT1284 devices are designed for asynchronous two-way communication between data buses. The control function minimizes external timing requirements.

The devices allow data transmission in either the A-to-B or the B-to-A direction for bits 1, 2, 3, and 4, depending on the logic level at the direction-control (DIR) input. Bits 5, 6, and 7, however, always transmit in the A-to-B direction.

The output drive for each mode is determined by the high-drive (HD) control pin. When HD is high, the high drive is delivered by the totem-pole configuration, and when HD is low, the outputs are open drain. This meets the drive requirements as specified in the IEEE 1284-I (level-1 type) and the IEEE 1284-II (level-2 type) parallel peripheral-interface specification.

ORDERING INFORMATION

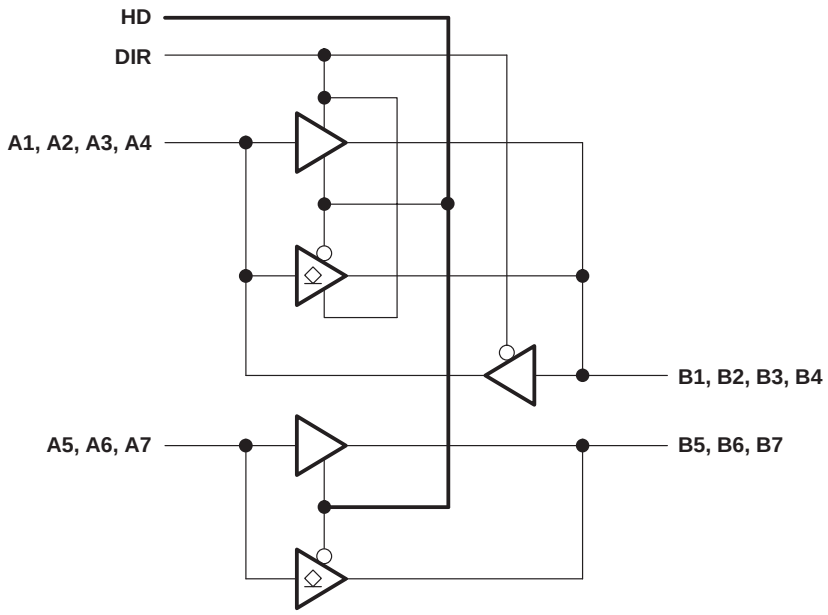
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC − DW	Tube	SN74ACT1284DW	ACT1284
		Tape and reel	SN74ACT1284DWR	
	SOP − NS	Tape and reel	SN74ACT1284NSR	ACT1284
	SSOP − DB	Tape and reel	SN74ACT1284DBR	AU284
	TSSOP − PW	Tube	SN74ACT1284PW	AU284
		Tape and reel	SN74ACT1284PWR	
−55°C to 125°C	CDIP − J	Tube	SNJ54ACT1284J	SNJ54ACT1284J
	CFP − W	Tube	SNJ54ACT1284W	SNJ54ACT1284W
	LCCC − FK	Tube	SNJ54ACT1284FK	SNJ54ACT1284FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		OUTPUT	MODE
DIR	HD		
L	L	Open drain	A to B: Bits 5, 6, 7
		Totem pole	B to A: Bits 1, 2, 3, 4
L	H	Totem pole	B to A: Bits 1, 2, 3, 4 and A to B: Bits 5, 6, 7
H	L	Open drain	A to B: Bits 1, 2, 3, 4, 5, 6, 7
H	H	Totem pole	A to B: Bits 1, 2, 3, 4, 5, 6, 7

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
B-port input and output voltage range, V_I and V_O (see Notes 1 and 2) . . . . . −2 V to 7 V
A-port input and output voltage range, V_I and V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package . . . . . 70°C/W
DW package . . . . . 58°C/W
NS package . . . . . 60°C/W
PW package . . . . . 83°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The ac input voltage pulse duration is limited to 20 ns if the input voltage goes more negative than −0.5 V.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			SN54ACT1284		SN74ACT1284		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.7	5.5	4.7	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Open-drain output voltage	HD low	0	5.5	0	5.5	V
I_{OH}	High-level output current	B port, HD high		−14		−14	mA
		A port		−4		−4	
I_{OL}	Low-level output current	B port		14		14	mA
		A port		4		4	
T_A	Operating free-air temperature		−55	125	0	70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

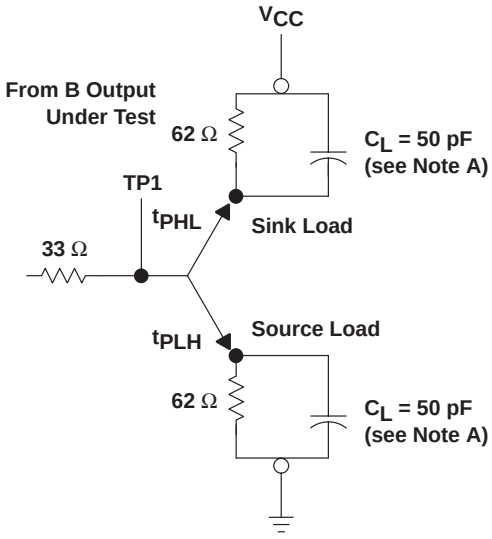
PARAMETER		TEST CONDITIONS	V_{CC}†	SN54ACT1284			SN74ACT1284			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{hys}	Input hysteresis	$V_{IT+} - V_{IT-}$ for all inputs	5 V	0.4			0.4			V
			4.7 V	0.2			0.2			
V_{OH}	B port	I_{OH} = −14 mA	4.7 V	2.4			2.4			V
	A port	I_{OH} = −50 µA	MIN to MAX	V_{CC}−0.2			V_{CC}−0.2			
		I_{OH} = −4 mA	4.7 V	3.7			3.7			
V_{OL}	B port	I_{OL} = 14 mA	4.7 V			0.4			0.4	V
	A port	I_{OL} = 50 µA				0.2			0.2	
		I_{OL} = 4 mA				0.4			0.4	
I_I		$V_I = V_{CC}$ or GND	5.5 V			±1			±1	µA
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			±20			±20	µA
I_{off}	B port	V_I or $V_O \le 7$ V	0 V			±100			±100	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			1.5			1.5	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4			4		pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12			12		pF
Z_O	B port	I_{OH} = −20 mA, I_{OH} = −50 mA	5 V	8		30	8		30	Ω

† For I/O ports, the parameter I_{OZ} includes the input leakage current I_I.
‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

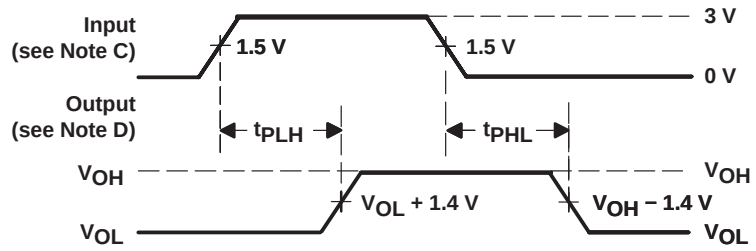
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	SN54ACT1284		SN74ACT1284		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	Totem pole	A or B	B or A	1	20	1	20	ns
t_{PHL}				1	20	1	20	
SR	Totem pole	B output		0.05	0.4	0.05	0.4	V/ns
t_{pd}(EN)	Totem pole	HD	B	1	20	1	20	ns
t_{pd}(DIS)				1	20	1	20	
t_r, t_f	Open drain	A	B		120		120	ns

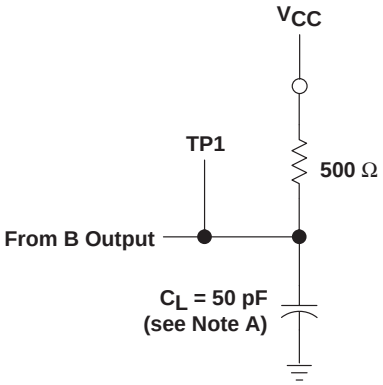
PARAMETER MEASUREMENT INFORMATION



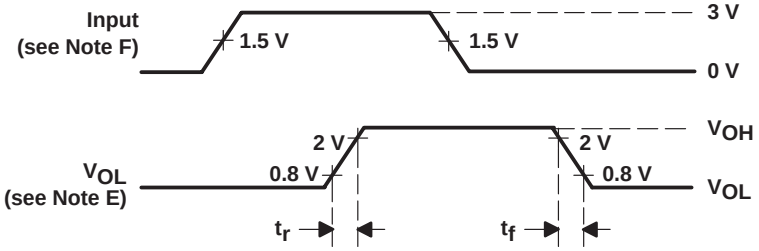
A-TO-B LOAD (totem pole)



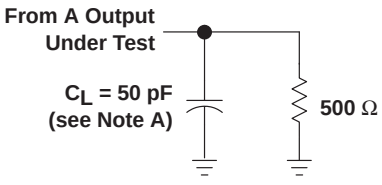
VOLTAGE WAVEFORMS MEASURED AT TP1
PROPAGATION DELAY TIMES (A to B)



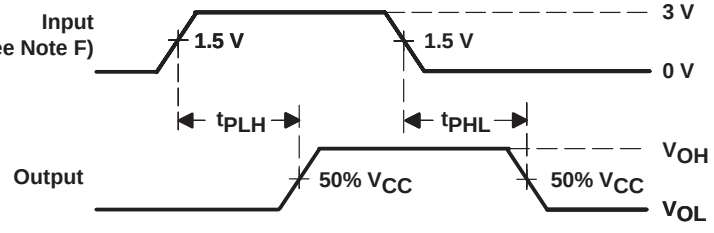
A-TO-B LOAD (open drain)



VOLTAGE WAVEFORMS MEASURED AT TP1 (B SIDE)



B-TO-A LOAD (totem pole)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)

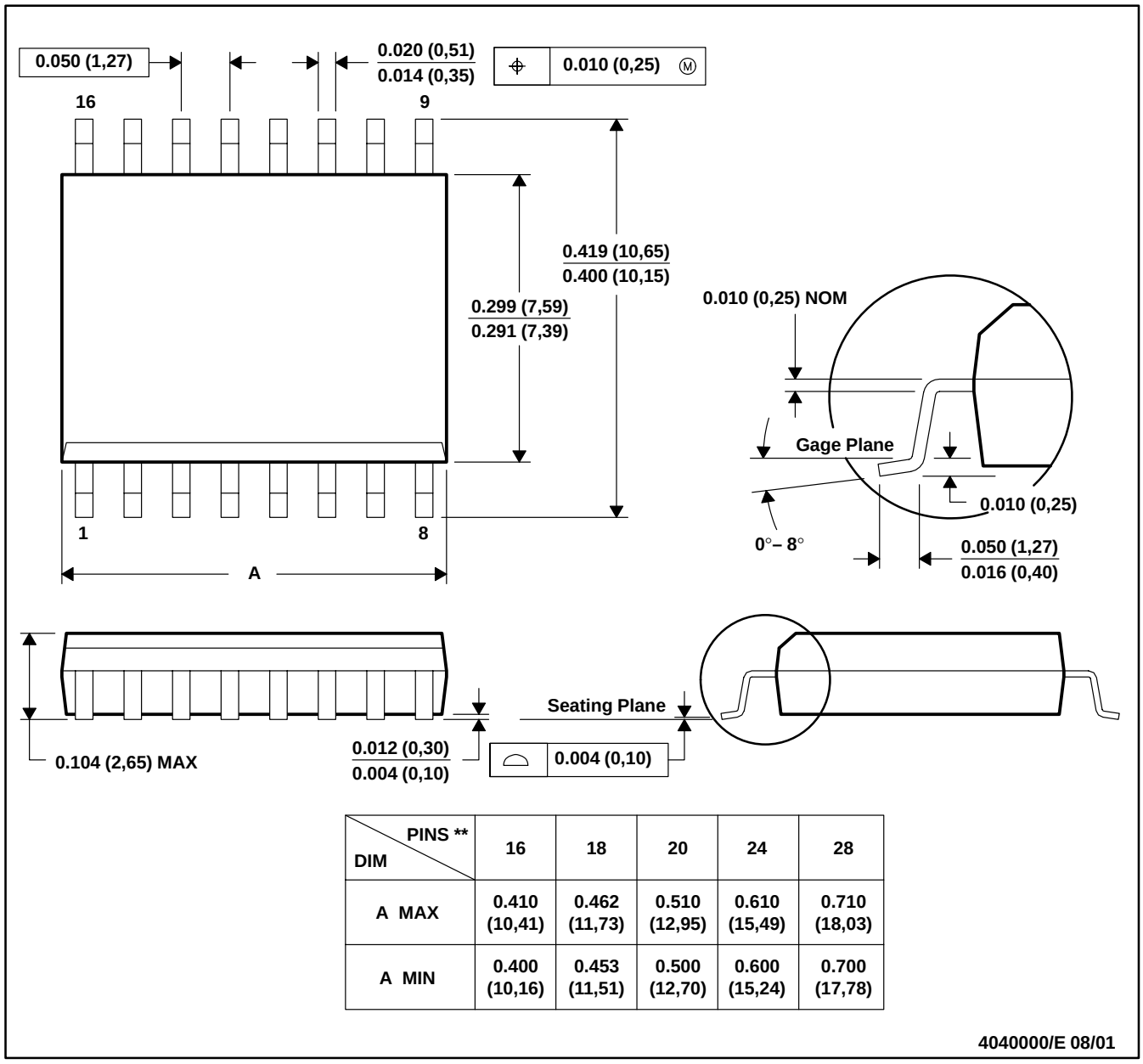
NOTES: A. CL includes probe and jig capacitance.
B. The outputs are measured one at a time with one transition per measurement.
C. Input rise and fall times are 3 ns, 150 ns < pulse duration <10 μs for both low-to-high and high-to-low transitions.
D. Slew rate is defined as 10% and 90% of the transition times.
E. Rise and fall times, open drain, are <120 ns.
F. Input rise and fall times are 3 ns.

Figure 1. Load Circuits and Voltage Waveforms

MSOI003E – JANUARY 1995 – REVISED SEPTEMBER 2001

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

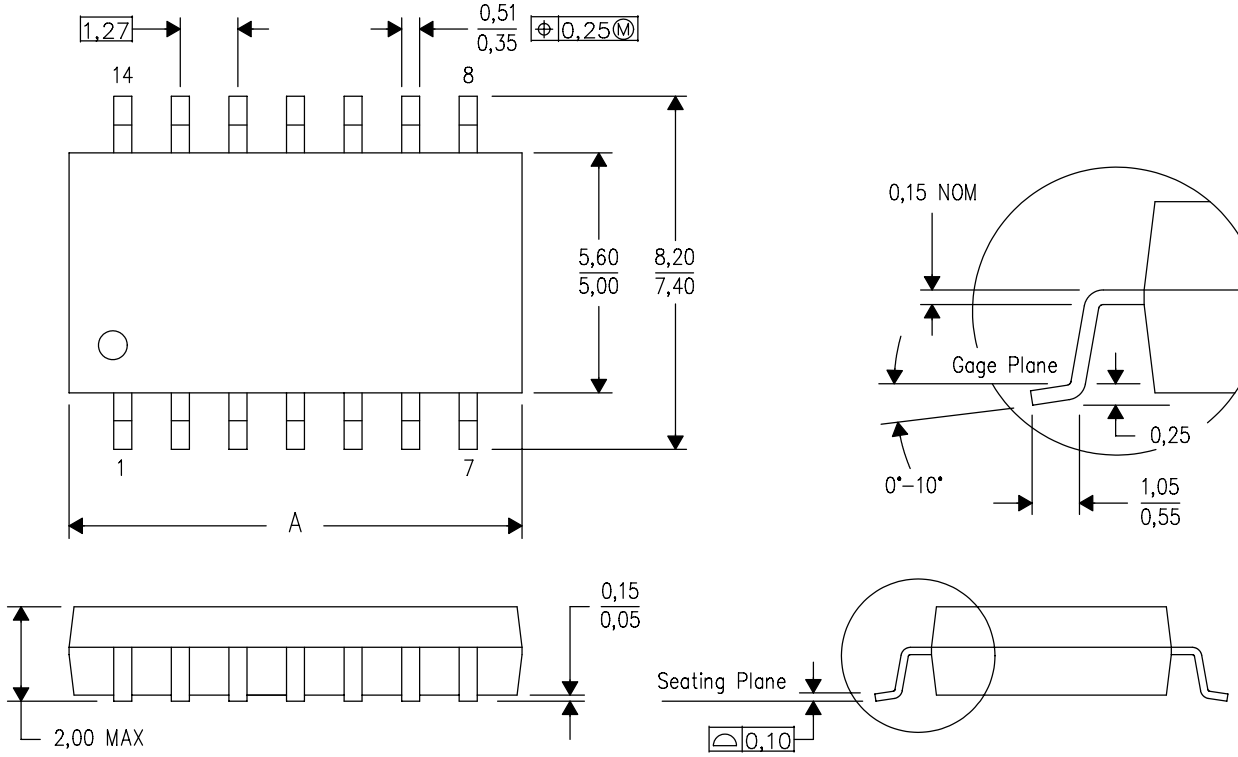
4040000/E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

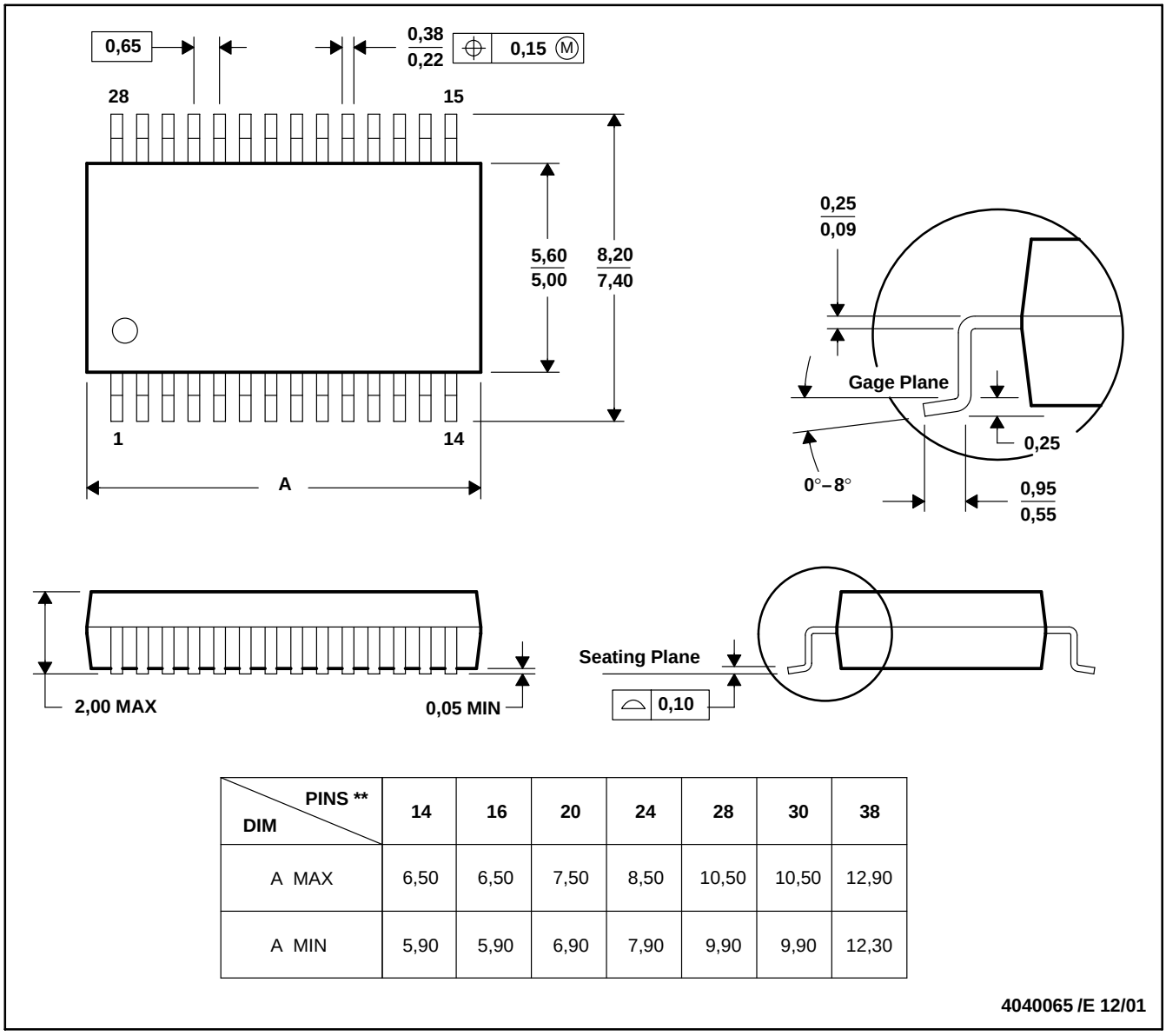
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



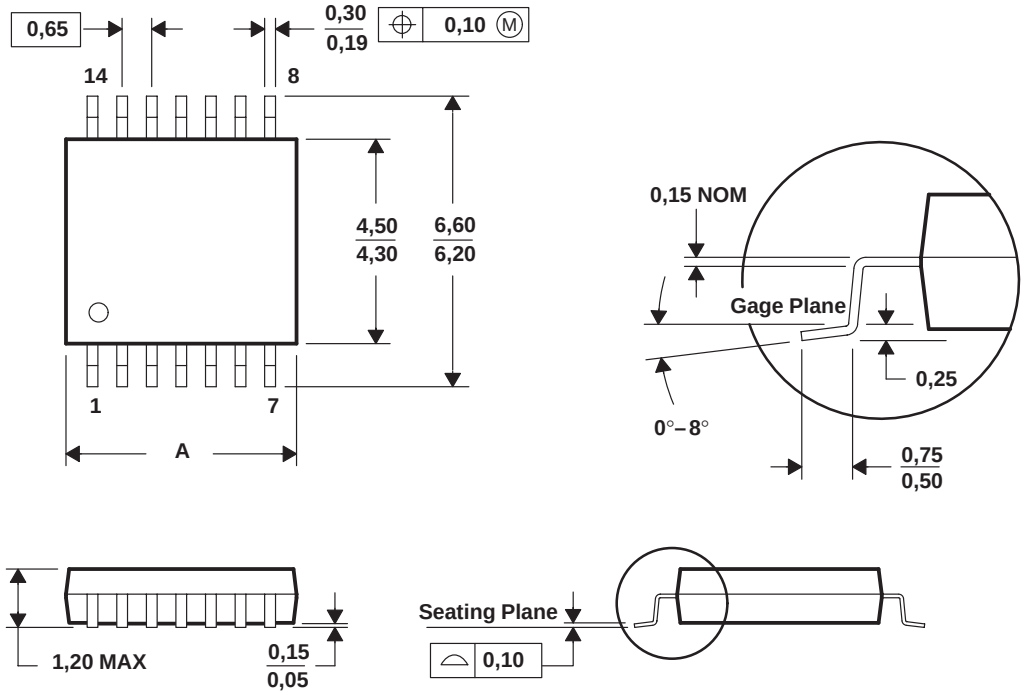
DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265